2. The non-volatile semiconductor memory device according to claim 1, wherein the second silicon nitride layer is formed by carrying, over a surface of the substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

Please replace the text of claim 3 with the following text:

3. The non-volatile semiconductor memory device according to claim 1, wherein a quantity of hydrogen content of the first silicon nitride layer is $10^{21}/cm^3$ or more.

Please replace the text of claim 4 with the following text:

4. The non-volatile semiconductor memory device according to claim 1, wherein a quantity of hydrogen content of the second silicon nitride layer is $10^{19}/cm^3$ or more.

Please replace the text of claim 5 with the following text:

5. A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on the semiconductor substrate, and a control gate provided through an inter-layer insulating layer on the floating gate,

wherein the inter-insulating layer comprises:

a silicon oxide layer contiguous to the floating gate and formed by a CVD method; and

a silicon nitrate layer deposited on the silicon oxide layer, the silicon oxide layer having a lower trap density than that of the silicon nitride layer.

Please replace the text of claim 6 with the following text:

6. The non-volatile semiconductor memory device according to claim 5, wherein the silicon oxide layer is deposited by carrying, over a surface of the substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

Please replace the text of claim 7 with the following text:

7. A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on the semiconductor substrate, and a control gate provided through an inter-layer insulating layer on the floating gate,

wherein the inter-insulating layer includes:

a silicon oxide layer contiguous to the floating gate; and

a silicon oxide layer deposited on the silicon oxide layer and having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less.

Please replace the text of claim 8 with the following text:

8. The non-volatile semiconductor memory device according to claim 7, wherein the silicon oxide layer is deposited by carrying, over a surface of the substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

Please replace the text of claim 9 with the following text:

9. A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory having a floating gate provided through a tunnel insulating layer on the semiconductor substrate, and a control gate provided through and inter-layer insulating layer on the floating gate,

wherein the inter-insulating layer includes:

a silicon oxide layer serving as a layer contiguous to at least one of the floating gate and the control gate, and having a lower trap density than that of a silicon nitride layer formed by a CVD method.

Please replace the text of claim 10 with the following text:

10. The non-volatile semiconductor memory device according to claim 9, wherein the silicon nitride layer is formed by carrying, over a surface of the substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

Please replace the text of claim 11 with the following text:

11. The non-volatile semiconductor memory device according to claim 9, wherein the silicon nitride layers are so double-layered as to be contiguous to both of the floating gate and the control gate, and

a silicon oxide layer is interposed in between the double-layered silicon nitride layers.

Please replace the text of claim 12 with the following text:

12. The non-volatile semiconductor memory device according to claim 9, wherein the silicon nitride layers are so double-layered as to be contiguous to both of the floating gate and the control gate, and

A stacked layer consisting of a silicon oxide layer and a silicon nitride layer formed by a CVD method is interposed in between the double-layered silicon nitride layers.

Please replace the text of claim 13 with the following text:

13. The non-volatile semiconductor memory device according to claim 9, wherein the silicon nitride layer is provided only on the side contiguous to the floating gate, and

a silicon oxide layer and a stacked layer consisting of a silicon nitride layer and a silico oxide layer which are foamed by the CVD method, are provided on the silicon nitride layer.

Please replace the text of claim 14 with the following text:

14. A non-volatile semiconductor memory device comprising:

a semiconductor substrate, and

a memory cell having a floating gate provided through a tunnel insulating layer on the semiconductor substrate, and a control gate provided through an inter-layer insulating layer on said floating gate,

Wherein the inter-insulating layer includes:

a silicon oxide layer serving as a layer contiguous to at least one of the floating gate and the control gate, and having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less.

Please replace the text of claim 15 with the following text:

15. The non-volatile semiconductor memory device according to claim 14, wherein the silicon nitride layer is formed by carrying, over a surface of the substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

Please replace the text of claim 16 with the following text:

16. The non-volatile semiconductor memory device according to claim 14, wherein the silicon nitride layers are so double-layered as to be contiguous to both of the floating gate and said control gate, and

a silicon oxide layer is interposed in between the double-layered silicon nitride layers.

Please replace the text of claim 17 with the following text:

17. The non-volatile semiconductor memory device according to claim 14, wherein the silicon nitride layers are so double-layered as to be contiguous to both of the floating gate and the control gate, and

a stacked layer consisting of a silicon oxide layer and a silicon nitride layer formed by a CVD method is interposed in between the double-layered silicon nitride layers.

Please replace the text of claim 18 with the following text:

18. The non-volatile semiconductor memory device according to claim 14, wherein the silicon nitride layer is provided only on the side contiguous to the floating gate, and

a silicon oxide layer and a stacked layer consisting of a silicon nitride layer and a silicon oxide layer which are formed by the CVD method, are provided on the silicon nitride layer.

REMARKS

The Office Action mailed March 28, 2001 has been carefully reviewed and the foregoing amendments and the following remarks are made in response thereto.

Claims 5, 6, 11, 12, 16 and 17 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Claims 1-4 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,661,056 to Takeuchi, IEEE Article of June 1, 1988 to Klein et al. [hereinafter "Klein"], Japanese Reference JP 358106873A to Yamada [hereinafter "Yamada"] and IEEE